Electroluminescent, Polycrystalline Cadmium Selenide Nanowire Arrays

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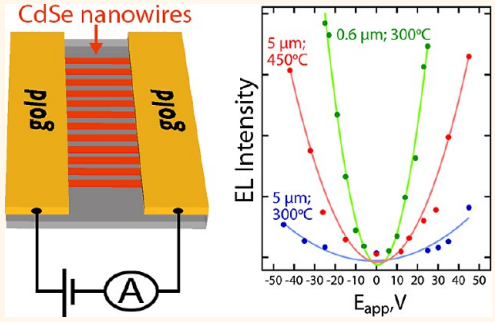
ABSTRACT Electroluminescence (EL) from nanocrystalline CdSe (*nc*-CdSe) nanowire arrays is reported. The n-type, *nc*-CdSe nanowires, 400−450 nm in width and 60 nm in thickness, were synthesized using lithographically patterned nanowire electrodeposition, and metal−semiconductor−metal (M−S−M) devices were prepared by the evaporation of two gold contacts spaced by either 0.6 or 5 μm. These M−S−M devices showed symmetrical current voltage curves characterized by currents that increased exponentially with applied voltage bias. As the applied biased was increased, an increasing number of nanowires within the array "turned on", culminating in EL emission from 30 to 50% of these nanowires at applied voltages of 25−30 V. The spectrum of the emitted light was broad and centered at 770 nm, close to the 1.74 eV (712 nm) band gap of CdSe. EL light emission occurred with an external quantum efficiency of 4×10^{-6} for devices with a 0.60 μm gap between the gold contacts and 0.5×10^{-6} for a 5 μm gap—values similar to those reported for M−S−M devices constructed from single-crystalline CdSe nanowires. Kelvin probe force microscopy of 5 μm *nc*-CdSe nanowire arrays showed pronounced electric fields at the gold electrical contacts, coinciding with the location of strongest EL light emission in these devices. This electric field is implicated in the Poole−Frenkel minority carrier emission and recombination mechanism proposed to account for EL light emission in most of the devices that were investigated.



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Light-emitting devices based upon semiconductor nanowires were first described by Lieber and co-workers in 2001.[1,2] Since then, a variety of nanowire-based architectures have been explored for light emission including single nanowires or arrays of nanowires,[3−6] core−shell heterostructures,[7−11] crossed nanowire p-n junctions,[12−14] and nanowire arrays interfaced to films.[15−19] Although fundamental physical and device fabrication challenges remain to qualify them for many future applications in integrated nanophotonic systems,[17] a purely practical problem is the absence of general methods for manipulating semiconductor nanowires so that they may be integrated into electrical circuits. The "nanowire integration problem" exists because semiconductor nanowires cannot be synthesized directly at the required location and with the correct orientation within an electrical circuit. In fact, most methods for synthesizing semiconductor nanowires produce an orientationally disordered powder either directly, as in solution phase synthetic methods, or as a consequence of the removal of oriented nanowires from a growth substrate as, for example, in vapor−liquid−solid (VLS) growth.[20−28]

The nanowire integration problem has motivated the development of high-throughput methods for incorporating nanowires from powders into electrical circuits: Capasso and co-workers[29] have described a method whereby electrical contacts are established transversely, across the short axis of ZnO nanowires. EL light emission from these structures was also characterized in that work.[29] Javey and co-workers[30] fabricated nanowire photodiodes using contact printing.[31−33] Heath and co-workers[34] stamped linear arrays of silicon nanowires onto adhesive-coated dielectrics. Lieber *et al.*[35] produced ensembles of uniaxially oriented nanowires and layers of crossed nanowires and showed that photolithography could be used to pattern a surface with single oriented nanowire layers or multilayers.[35] Yang *et al.* used programmed dipping of substrates to prepare aligned ensembles of

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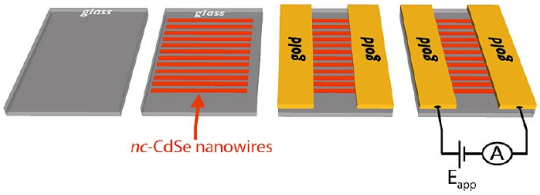

Figure 1. Schematic diagram depicting the fabrication of light-emitting M−S−M junctions starting with an array of *nc*-CdSe nanowires prepared using lithographically patterned nanowire electrodeposition.

nanowires.[36] Even nanowire layers in which nanowires have some degree of misorientation have proven to be applicable in a variety of different types of devices.[37] Bayindir and co-workers[38,39] have demonstrated a process of mechanically aligning ensembles of nanowires on top of prefabricated metal electrical contacts to produce photodetectors.

Instead of positioning nanowires within prefabricated contacts, an alternative approach is to synthesize the nanowires first, in a predetermined position and orientation on a dielectric substrate, and then pattern electrical contacts as shown schematically in Figure 1. Lithographically patterned nanowire electrodeposition (LPNE)[40−42] can be used to pattern arrays of thousands of CdSe nanowires,[43−45] for example, across ≈1−5 cm^2 areas onto a variety of dielectric substrates. A disadvantage of this approach is the fact that these nanowires are nanocrystalline, not single crystalline. In this paper, we explore the feasibility of the scheme shown in Figure 1 for patterning electroluminescent (EL), nanocrystalline CdSe (*nc*-CdSe) nanowire arrays.

CdSe is a direct band gap semiconductor (E_g = 1.75 eV) that has applications in electrical and photonic devices including photodetectors,[43,44,46−48] light-emitting diodes,[4,5,16] solar photovoltaics,[49−52] and field-effect transistors.[28,45,53−57] Recently,[45] we have demonstrated that field-effect transistors based upon lithographically patterned *nc*-CdSe nanowire arrays can be prepared, but the emission of light from polycrystalline semiconductor nanowires has not been studied at all, to our knowledge; all CdSe nanowire light-emitting devices have been prepared using single-crystalline nanowires.[4,5,12,16] In this work, lithographically patterned nanowire electrodeposition (LPNE) method is used to fabricate arrays of hundreds of nanocrystalline CdSe (*nc*-CdSe) nanowires with dimensions of 400−450 nm (*w*) × 60 nm (*h*) and lengths of millimeters. We compare the EL properties of *nc*-CdSe nanowires that were subjected to either of two post-thermal annealing processes: 300 °C × 4 h in nitrogen, and 450 °C × 1 h in nitrogen. In addition, for the lower annealing temperature, the influence of the electrically isolated length of the nanowires is evaluated by comparing gold contacts with a 5 μm spacing to contacts with a gap of ≈0.6 μm, fabricated using a shadow/etching method described here. EL light emission was observed for all *nc*-CdSe nanowire arrays prepared here, and the properties of this light emission are disclosed in this study.

RESULTS AND DISCUSSION

Synthesis of *nc*-CdSe Nanowires Using LPNE and Characterization. *nc*-CdSe nanowires on glass and SiO_2/Si substrates were prepared by electrodeposition using the LPNE method[40−42] as previously described.[43−45] Our procedure exploits the scanning electrodeposition/stripping method pioneered by Sailor *et al.*,[58] resulting in near stoichiometric *nc*-CdSe nanowires.[43,44,59,60] In this study, *nc*-CdSe nanowires were prepared in a linear array at 5 μm pitch (Figure 2a) and four voltammetric scans were used for nanowire electrodeposition. As-deposited *nc*-CdSe nanowires were then thermally annealed using either of two processes: (1) 300 °C × 4 h in N_2 or (2) 450 °C × 1 h in N_2.

Grazing incidence X-ray diffraction (GIXRD) patterns were acquired for thousands of *nc*-CdSe nanowires after these thermal annealing treatments. These patterns are characterized by three reflections assignable to a zinc blende structure (JCPDS 88-2346, Figure 2b). Application of the Scherrer equation[61] to the (111) reflection provides an estimate of the mean grain diameter of 9 nm for nanowires annealed at 300 °C × 4 h, and this value increases to 32 nm for nanowires annealed at 450 °C × 1 h. In our previous work,[43−45] we have also observed a cubic structure for CdSe nanowires annealed at 300 °C, but the fact that the cubic crystal structure is retained up to 450 °C is interesting and unexpected in view of the fact that a phase transition from cubic to hexagonal has been observed for CdSe in the 350−400 °C range.[62−65] In prior work, X-ray photoelectron spectroscopy of CdSe nanowires prepared using this procedure and annealed at 300 °C × 4 h shows a cadmium/selenium ratio of 1.08.[44]

Raman spectra were also acquired both for *nc*-CdSe nanowires annealed at 300 °C and those annealed at 450 °C (Figure 2c). Both sets of annealing conditions produced spectra showing a strong transition at 204−206 cm^{-1} that is assigned to the longitudinal optical (LO) phonon mode in accordance with prior work on CdSe.[66−68] However, for nanowires annealed at 450 °C, a narrower peak is observed, suggesting a higher degree of crystallinity and homogeneity for these samples (Figure 2c). The influence of the annealing temperature is also apparent in the surface morphology of the *nc*-CdSe nanowires seen in SEM images (Figure 2d,e). Individual grains are not discernible for nanowires annealed at 300 °C (Figure 2d); however, these nanowires show a "laminated" appearance in which individual CdSe layers, each produced by a single cycle of the cyclic deposition process, are stacked along the growth direction. In SEM images of *nc*-CdSe nanowires annealed at 450 °C (Figure 2e), on the other hand, this laminated texture is no longer present and individual grains are now readily observable, ranging in diameter from 30 to 50 nm. This is

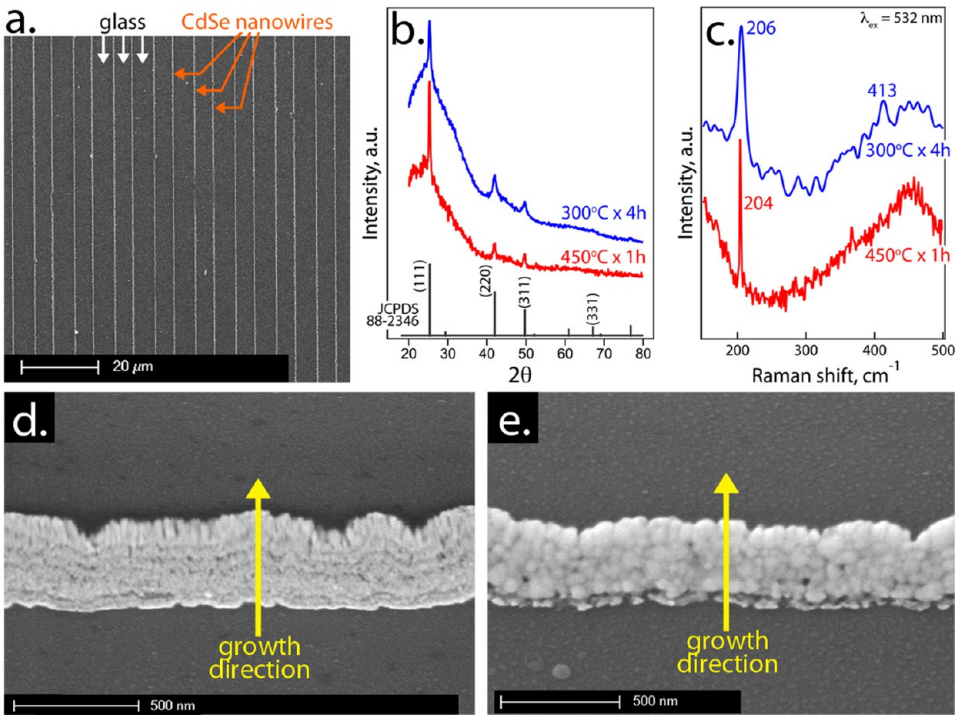

Figure 2. Structural characterization of annealed *nc*-CdSe nanowires prepared by LPNE. (a) Low-magnification SEM image of *nc*-CdSe nanowires deposited at 5 μm pitch. These arrays were used for characterization by SEM, grazing incidence X-ray diffraction (GIXRD), and Raman spectroscopy. (b) GIXRD patterns of *nc*-CdSe nanowires subjected to two thermal annealing treatments: (blue trace) 300 °C × 4 h in N_2, and (red trace) 450 °C × 1 h in N_2. The mean grain diameter derived from the line width of the (111) reflection using the Scherrer equation is 9 nm (300 °C × 4 h) and 32 nm (450 °C × 1 h). (c) Raman scattering spectra (λ_{ex} = 532 nm) for the same two annealing treatments shown in (b). (d) High-magnification SEM image of *nc*-CdSe nanowires thermally annealed at 300 °C for 4 h. The growth direction of the nanowire is indicated. (e) High-magnification SEM image of *nc*-CdSe nanowires thermally annealed at 450 °C for 1 h.

consistent with the mean grain diameter of 32 nm estimated for these samples using GIXRD.

Electroluminescence (EL) in *nc*-CdSe Nanowires. The electroluminescence properties of arrays of 350 *nc*-CdSe nanowires, electrodeposited at 5 μm pitch on glass, were probed in this study using an optical microscope outfitted with an intensified charge-coupled device (CCD) camera and an f4 spectrograph. Two electrode spacings were evaluated in this study: 5 and 0.60 μm. Gold electrodes were prepared with a 0.6 μm spacing as shown in Figure 3c using a novel shadow mask process (Figure 3a). Conventional vacuum evaporation, photolithography, and lift-off were used to prepared contacts with a 5 μm spacing (Figure 3b).

Current *versus* voltage ($|I|-V$) curves were approximately symmetrical about E_{app} = 0 V for all three of the devices explored in this study (Figure 4a). The pronounced curvature of these $|I|-V$ curves is a characteristic of M–S–M devices that incorporate Schottky barriers at both contacts,[69−71] including those prepared from polycrystalline CdSe films,[72−75] and has also been reported for M–S–M structures that incorporate semiconducting nanowires.[76,77] The ohmic resistance, R, of the *nc*-CdSe nanowires in these two devices cannot be accurately measured from these $I-V$ curves, but a minimum value for R can be obtained from dV/dI evaluated at high E_{app} values.[78] Using this estimate, the electrical resistance of the *nc*-CdSe nanowires annealed at 300 °C for 4 h is ~20–30 times higher than those annealed at 450 °C for 1 h. The lower resistance of the *nc*-CdSe nanowires prepared at 450 °C could be a manifestation of the larger grain diameter in the *nc*-CdSe (Figure 2b) or a higher dopant density in these samples, and the relative weighting of these two contributions cannot be determined from our data. Several mechanisms can account for current transport across these M–S–M devices including Schottky emission,[69,70] Poole–Frenkel emission,[69,70,79,80] thermionic emission,[78,81] thermionic field emission,[78,81] Fowler–Nordheim tunneling,[70] and space-charge-limited injection.[70,79,80] Plots of ln I *versus* $\sqrt{V}$ are approximately linear (Figure 4b), as expected for conduction limited by either Schottky emission (eq 1) or Poole–Frenkel emission (eq 2):[70,79,80]

$$I = AT^2 \exp\left(-\frac{\phi_s}{kT}\right) \exp\left(\frac{\beta_s V^{1/2}}{kTd^{1/2}}\right) \quad (1)$$

$$I = I_0 \exp\left(\frac{\beta_{pf} V^{1/2}}{kTd^{1/2}}\right) \quad (2)$$

where A is the Richardson constant, ϕ_s is the Schottky barrier height, d is the thickness of the semiconductor layer, I_0 is the low-field current, and β_s and β_{pf} are,

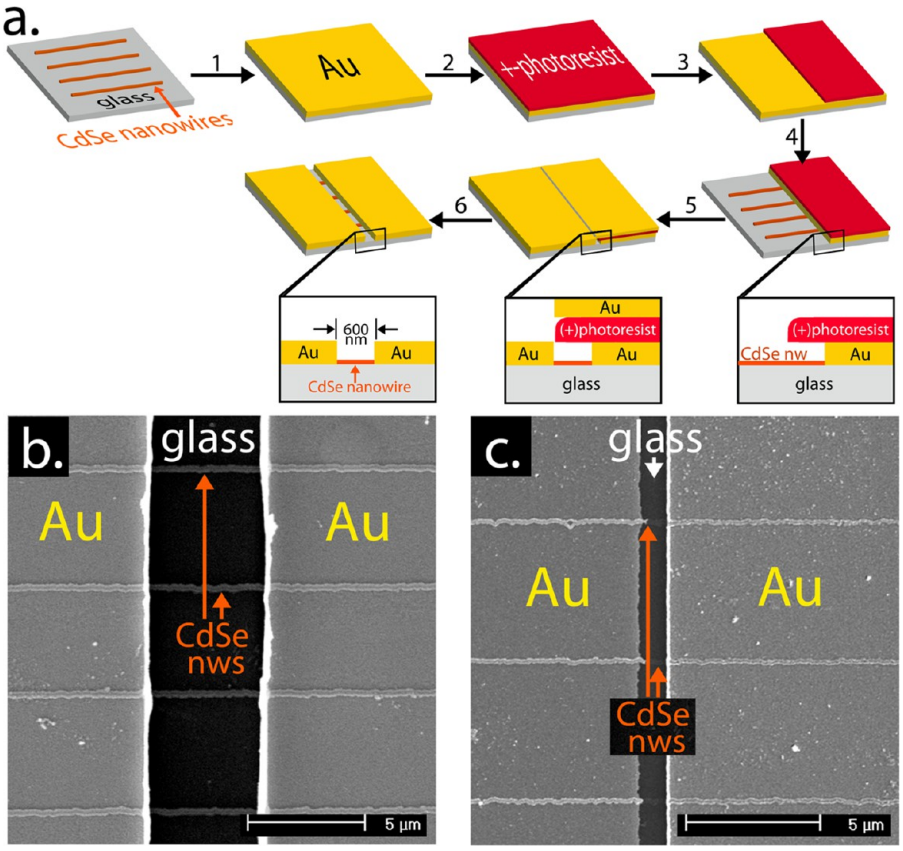

Figure 3. Fabrication of electroluminescent Au–*nc*-CdSe nanowire–Au arrays. (a) Process flow for the preparation by etching of a shadow mask enabling the preparation of evaporated gold contacts with a gap of 0.60–0.80 μm on *nc*-CdSe nanowire arrays. (b) SEM image of *nc*-CdSe nanowire array with 5 μm gold contacts, prepared using conventional photolithography and lift-off. (c) SEM image of *nc*-CdSe nanowire array with gold contacts spaced at ≈0.60 μm, prepared using the etching/shadow mask process shown in (a).

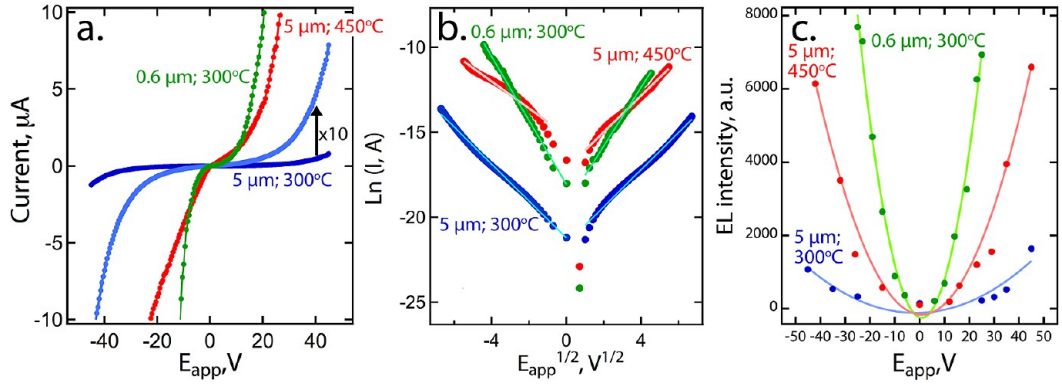

Figure 4. Current *versus* voltage data (a,b) and EL intensity *versus* voltage (c) for three light-emitting junctions.

respectively, the Schottky and Poole–Frenkel field-lowering coefficients.[70,80] Poole–Frenkel emission is known to be favored for materials having low mobilities, μ_{eff},[82−84] a condition that applies to these *nc*-CdSe nanowires where μ_{eff} is in the range from 10^{-4} to 10^{-5} cm^2/(V s).[45] If purely Poole–Frenkel emission is occurring, then $\beta_{pf} = (e^3)/(\pi\varepsilon_s)^{1/2}$. For $\varepsilon_s = 7.82 \times 10^{-11}$ F/m, the theoretically expected value for CdSe is $\beta_{pf} = 2.55 \times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$.[73] We measure β_{pf} ranging from 7.4×10^{-6} to 1.2×10^{-5} eV m$^{1/2}$ V$^{-1/2}$—close to the β_{pf} values obtained previously for CdSe (Table 1). Although the participation of other mechanisms cannot be ruled out, we conclude that it is likely that Poole–Frenkel emission is a major contributor to transport across these nanowire junctions.

Like the *I*–*V* curves, the EL emission intensity also increases nonlinearly with increasing E_{app} (and *I*), and this behavior is symmetric for both polarities (Figure 4c). Very similar data have been reported by Doh *et al.*[4] for M–S–M junctions prepared from single-crystalline CdSe nanowires. Since the devices investigated here consist of 350 Au–*nc*-CdSe nanowire–Au

junctions connected electrically in parallel (Figure 5a), it is useful to ask, what fraction of these devices contribute to the observed EL emission measured in Figure 4c? This question can be addressed by imaging these arrays during the application of an applied bias.

TABLE 1. Comparison of β_{pf} Values for CdSe Films, Nanostructures, and Nanocrystalline Nanowires

description	β_{pf}[a] eV m$^{1/2}$ V$^{-1/2}$	ref
CdSe thin film	2.7×10^{-5}	73
CdSe quantum dots	1.1×10^{-5}	95
CdSe thin film	$4.4-4.9 \times 10^{-4}$	96
nc-CdSe nanojunction electrodeposited at 20 °C	4.2×10^{-5}	93
nc-CdSe nanojunction electrodeposited at 75 °C	9×10^{-5}	93
CdSe (calculated)[b]	2.55×10^{-5}	73
nc-CdSe nw arrays:		
annealed 300 °C × 4 h	7.0×10^{-6}	this work
annealed 450 °C × 1 h	7.4×10^{-6}	this work
annealed 300 °C × 4 h	1.2×10^{-6}	this work

[a] β_{pf} is the Poole–Frenkel field lowering coefficient, from eq 2. [b] $\beta_{pf} = (e^3)/(\pi\varepsilon_s)^{1/2}$, where, for CdSe, $\varepsilon_s = 7.82 \times 10^{-11}$ F/m.[73]

In Figure 5b are shown 40 μm × 330 μm optical images of these junctions as a function of the total device current. With increasing E_{app} and I, the number of emissive nanowires increases. The intensity of EL emission from individual nanowires, however, increases for some devices and decreases for others. For 0.60 μm junctions, "blinking"—involving the turning off of emitting junctions and the turning on of dark junctions as E_{app} was monotonically increased—was often observed (Figure 5b, bottom). The fraction of emissive nanowire junctions varied from ≈30% for the 0.60 μm junctions to ≈50% for the 5 μm junctions and 300 °C × 4 h nanowires (Figure 5c).

Using these data, the external quantum efficiency (EQE) can be estimated[11,85]

$$\mathrm{EQE} = \frac{\text{photons emitted per second}}{\text{number of electrons injected per second}} = \frac{P_{opt}/h\nu}{I/e} \quad (3)$$

where P_{opt} is the measured optical power, h is Planck's constant, ν is the frequency of the emitted light, I is the

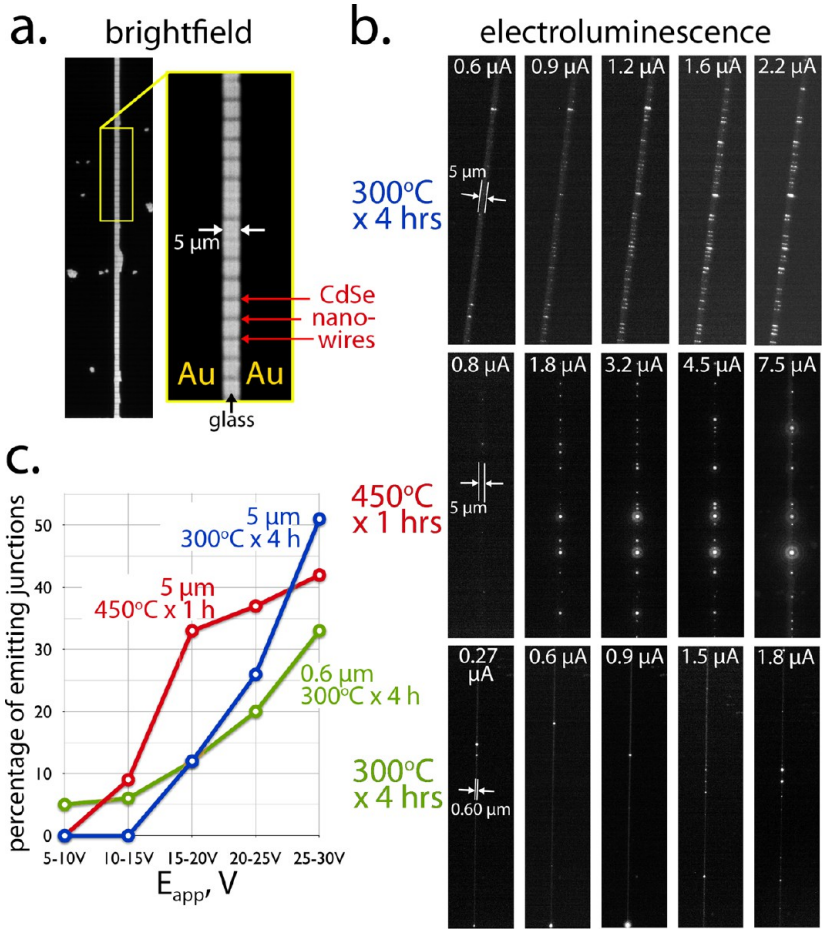

Figure 5. Optical micrographs of emissive *nc*-CdSe nanowire arrays. (a) Bright-field images for the 450 °C/1 h in the 5 μm gap array showing nanowires and gold electrodes. (b) EL for three *nc*-CdSe devices as indicated. In each image, the total current is indicated. The E_{app} values for these experiments, in parentheses, are as follows: 5 μm, 300 °C × 4 h, 0.6 μA (20 V), 0.9 μA (28 V), 1.2 μA (37 V), 1.6 μA (45 V), 2.2 μA (56 V); 5 μm, 450 °C × 1 h, 0.8 μA (12 V), 1.8 μA (16 V), 3.2 μA (23 V), 4.5 μA (29 V), 7.5 μA (35 V); 0.6 μm, 300 °C × 4 h, 0.27 μA (6 V), 0.6 μA (9 V), 0.9 μA (23 V), 1.5 μA (29 V), 1.8 μA (35 V). (c) Plot of the percentage of emissive nanowire junctions as a function of E_{app}.

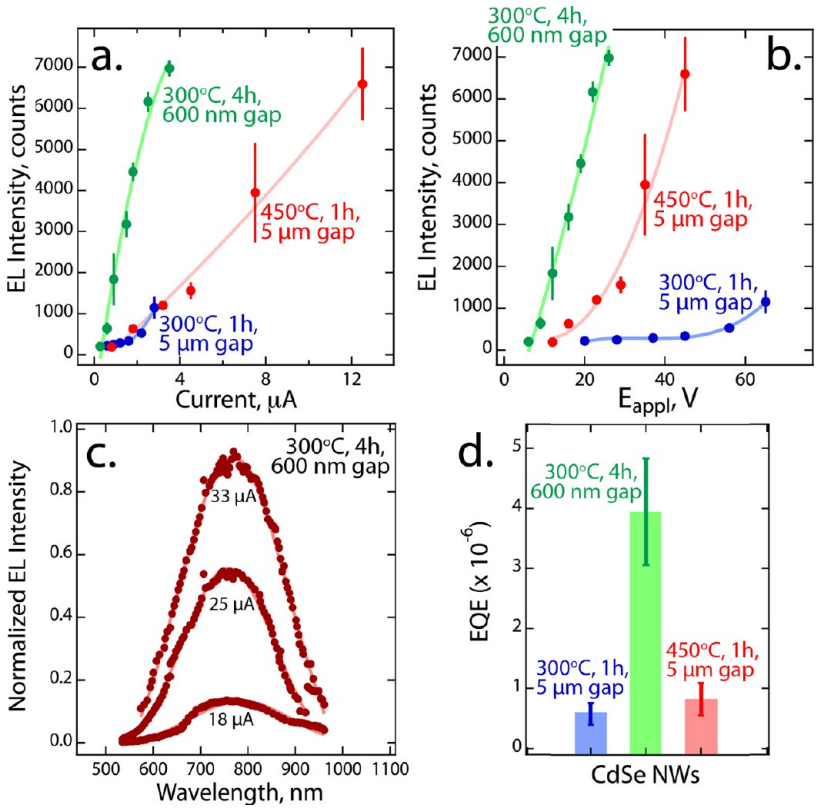

Figure 6. EL emission properties of arrays of 350 M–S–M junctions prepared from *nc*-CdSe nanowires. (a) EL emission intensity as a function of the total current for the three types of devices described in Figure 5. (b) EL emission intensity *versus* applied voltage, E_{app}. (c) EL emission spectra acquired for *nc*-CdSe nanowires annealed at 300 °C for 4 h using a 0.60 μm gap. (d) Mean external quantum efficiency (EQE) for the three types of devices. Devices that employed a 0.60 μm gap were more efficient than 5 μm devices by a factor of 5 or more.

TABLE 2. Comparison of Device Metrics for Nanowire and Nanorod Light-Emitting Junctions and Diodes

emissive element(s)[a]	device[b]	device length[c] (μm)	V_{th}[d] (V)	λ_{max}[e] (nm)	EQE[f]	ref
CdSe nr	MSM	0.030	1.75	750, 720	10^{-5}	5
CdSe nw	MSM	2–6	4	730	$(1–5) \times 10^{-6}$	4
CdSe nw + graphene	p-n	≈2–3	4	705	na	16
n-CdSe + p-Si nw	p-n	≈1	na	700	10^{-3}–10^{-2}	12
n-InP + p-InP nw	p-n	≈2	1.7	820	10^{-5}	1
GaN nw	n-i-n	na	3	900	10^{-8}	3
CdSe nw arrays:						
annealed 300 °C × 4 h	MSM	5	16(±5)	na	$6(\pm2) \times 10^{-7}$	this work
annealed 450 °C × 1 h	MSM	5	12(±1)	na	$8(\pm2) \times 10^{-7}$	this work
annealed 300 °C × 4 h	MSM	0.6	6.2(±0.5)	750–780	$4(\pm1) \times 10^{-6}$	this work

[a] Abbreviations: nr = nanorod, nw = nanowire. [b] Abbreviations: MSM = metal–semiconductor–metal, p-n = p-n junction photodiode, n-i-n = semiconductor–insulator–semiconductor junction. [c] The distance across the emissive element between the electrical contacts. [d] Threshold voltage for EL light emission. [e] Wavelength of maximum emission intensity. [f] External quantum efficiency.

current, and *e* is the elementary charge. Values ranging from $(6–8) \times 10^{-7}$ for the 5 μm devices to $4(\pm1) \times 10^{-6}$ for the 0.60 μm devices are thereby obtained. Thus, the 0.60 μm devices are more efficient by an order of magnitude, in spite of the fact that fewer emissive nanowires contribute to the overall EL. In previous work, devices based upon single emissive CdSe nanowires[5] and nanorods[4] show EQE values ranging from 10^{-5} to $(1–5) \times 10^{-6}$ (Figure 6d). This range, reported for single-crystalline CdSe nanorods, also encompasses the EQE values measured for the 0.60 μm devices described here (Table 2).

nc-CdSe nanowire arrays with 0.60 μm gaps also generate EL more power-efficiently than nominally identical nanowire arrays having 5 μm gaps (Figure 6a, b). One factor contributing to this power efficiency is the reduced ohmic resistance of the shorter nanowire which is reduced by the ratio 0.6/5.0; a factor of ≈1/8.

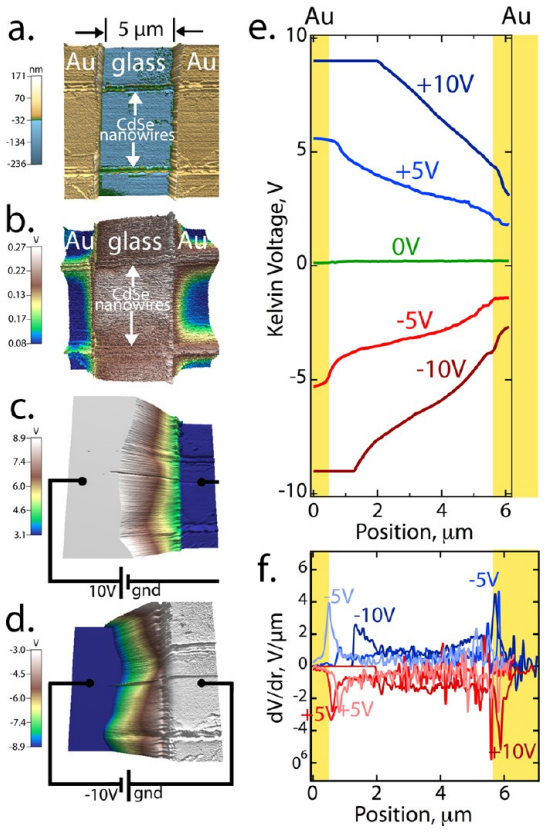

Figure 7. Noncontact AFM (nc-AFM) and Kelvin probe force microscopy (KPFM) images and potential measurements. (a) nc-AFM image of a 5−6 μm gap containing two nanowires. (b−d) KPFM images of the surface potential acquired at applied voltages, E_{app} = 0 V (a), +10 V (c, left *versus* right), and −10 V (d). Note that with the microscope amplifier saturated at ±8.9 V, larger voltages could not be measured. (e) Plots of the surface potential (e) and its gradient, d/dr, (f) measured along the axis of a CdSe nanowire for E_{app} = 0, ±5, and ±10 V, as indicated.

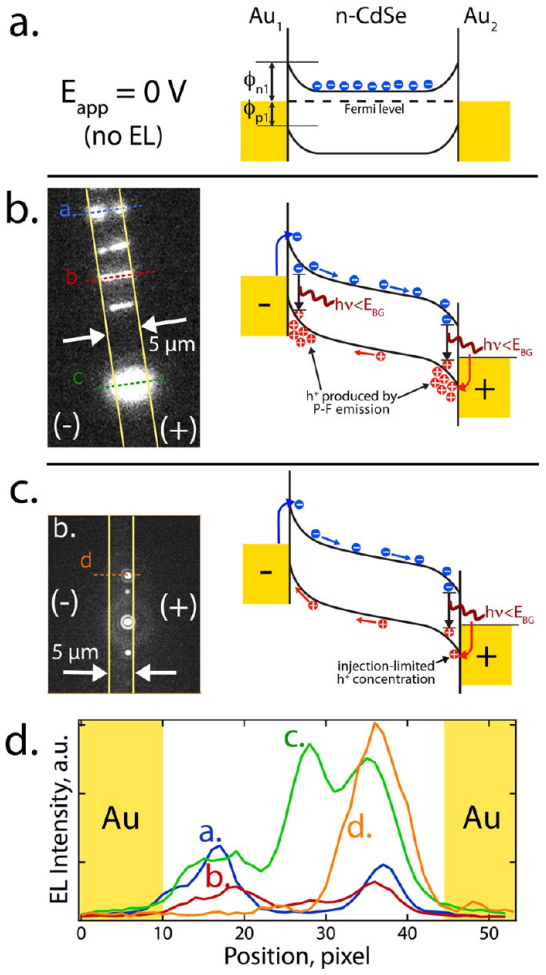

Figure 8. Spatial distribution of EL and proposed EL mechanisms. (a) For E_{app} = 0 V, no EL emission occurs because the hole concentration in the n-type *nc*-CdSe nanowire is negligible. (b) For 70% of the *nc*-CdSe nanowires investigated here, the application of a bias induces current flow, and for $E_{app} > E_{th}$ (Table 2), EL emission is observed near (with 1.5 μm) *both* gold contacts (plotted in d). This is consistent with EL caused by Poole−Frenkel minority carrier emission-limited recombination that is located in the high-field regions located near both gold electrodes (Figure 7), as depicted in the band diagram at right, (c) but 30% of the nanowires showed EL emission for $E_{app} > E_{th}$ that was restricted to the positive contact, as shown here (and plotted in d). This is consistent with EL caused by minority carrier injection-limited recombination, as depicted in the band diagram at right. (d) EL emission intensity as a function of position along the nanowire relative to the gold contacts, shown in yellow. The four traces, (a) − (d), correspond to the four devices indicated in the optical images above.

As seen in Figure 6a,b, EL is produced at lower currents and voltages in the 0.60 μm devices. Relative to single-crystalline nanowire emitters where the threshold voltage for EL emission, V_{th} = 1.75[4] or 4 V,[5] a V_{th} of 6 V (0.60 μm gap) or 12−16 V (5.0 μm gap) is observed, but it should be noted that, across all these devices, V_{th} is strongly correlated with the emitter length (Table 2). The higher EQE of the 0.60 μm arrays can be directly seen in Figure 6a where the same current of 3 μA produces 7−10 times the EL intensity for nominally identical *nc*-CdSe nanowires, in both cases prepared by annealing at 300 °C for 4 h. The acquisition of spectra for the EL was possible only for these brightest devices constructed with 0.60 μm gaps (Figure 6c). These spectra are characterized by a broad emission centered at a wavelength of 750−780 nm, red-shifted slightly from the 1.74 eV (712 nm) band gap of CdSe.

Before positing a mechanism for EL light emission, two other pieces of data must be taken into consideration. First, we exploited Kelvin probe force microscopy (KPFM)[86] to map the contact potential difference for 5 μm devices. Previous studies have exploited KPFM to investigate emissive semiconductor device structures[87,88] including two involving nanowire emissive elements.[4,89] A nc-AFM topographic image of a 10 μm × 10 μm region of a device (Figure 7a) shows the gold contacts and two *nc*-CdSe nanowires connected across a 6 μm gap. At E_{app} = 0 V, a KPFM map of the surface potential in the same region (Figure 7b) shows slight variations of ≈0.30 V from edge to edge. Application of a ±10 V bias to the device (Figure 7c,d) produces a sharp gradient in surface potential across the nanowires (Figure 7e) that is concentrated within 1 μm of

the contacts (Figure 7f). Second, an examination of optical micrographs shows that EL emission occurs in close proximity—within 1.5 μm—to one or both interfaces of the nanowire with the gold contacts (Figure 8). For 70% of the 2000 emissive nanowire junctions examined in this study, EL was observed at both gold contacts (Figure 8b,d). For the remaining 30% of the emissive junctions, EL was confined to the positive contact, irrespective of the polarity of the applied bias (Figure 8c,d).

Electroluminescence from M−S−M junctions has been attributed to a variety of mechanisms.[5,70,90−92] Our data implicate either of two mechanisms—one operating for devices where EL is localized at the positive contact ("anode emitters"), and a second that operates in the majority of devices where emission is observed simultaneously near both contacts ("bipolar emitters"). Both of these mechanisms assume that the *nc*-CdSe nanowires are n-type, as this has previously been established from FET measurements.[45] For anode emitters, the mechanism is the same as we have previously reported for *nc*-CdSe that is electrodeposited into gold nanogap structures[93]—minority carrier injection-limited recombination.[69] In this model, EL emission occurs when injected holes at the anode recombine radiatively with majority electrons in the vicinity of the contact. If EL emission is pseudo-first-order in injected holes, then we expect a linear dependence of EL intensity on current, approximately as observed (Figure 6a). Doh *et al.*[4] also observed localization of EL at a gold anode for single-crystalline CdSe nanowires, although they invoke a different mechanism to account for this EL.

Simultaneous EL emission at both contacts cannot occur by this mechanism since, at the cathode, charge injection involves electrons. In this case, we propose that the EL mechanism occurs by a Poole−Frenkel minority carrier emission and recombination process in which minority holes are "emitted" from shallow traps by a Schottky-like emission process. These holes are then available for radiative recombination with electrons to produce EL. Three observations support a Poole−Frenkel minority carrier emission and recombination model for this EL emission: (1) Current *versus* voltage curves conform to the predictions of Poole−Frenkel emission (Figure 4b). This is evidence, completely independent from the EL measurements, that P−F emission occurs in these nanowires. (2) EL emission at the contacts increases monotonically with increasing E_{app} for all the bipolar emitting junctions we probed, suggesting that the EL emission is strongly coupled to the electric field (Figures 4c, 5, and 6a,b). Finally, (3) KPFM (Figure 7) provides direct evidence for the presence of enhanced electric fields in the vicinity of both contacts.

CONCLUSIONS

The most important conclusion of this work is that *nc*-CdSe nanowires, lithographically patterned onto glass using the LPNE process, can produce EL. The quantum yield for light emission in these systems is low ($\approx 10^{-6}$), but it is similar to the EQEs measured for devices based upon single-crystalline CdSe nanowires.[4] The intensity of light emission and the number of emissive junctions both increased as a function of the applied voltage up to $E_{app} = 25-30$ V in this study. It is significant that at these high biases, up to 50% of the *nc*-CdSe M−S−M junctions showed EL emission. For 70% of the 2000 emissive nanowire junctions examined in this study, EL was observed at both gold contacts by a mechanism that we believe involves Schottky-like field ionization of trapped holes and subsequent radiative recombination of these holes with majority electrons near the electrical contacts where KPFM shows these fields are the largest. We conclude that, with some refinement, electrodeposition might be used in conjunction with lithographic patterning to produce nanometer scale light emitters for a variety of technological applications.

EXPERIMENTAL SECTION

Chemicals and Materials. Cadmium sulfate ($CdSO_4 \cdot 8H_2O$, 98+%), selenium oxide (SeO_2, 99.9+%), iodine (I_2, 99.8%), and chromium etchant were used as received from Sigma-Aldrich. Sulfuric acid (ULTREX ultrapure) was purchased from J.T. Baker. Potassium iodide (KI, 99+%) and acetone were used as received from Fisher (ACS Certified). Positive photoresist (Shipley, S1808) and developer (Shipley, MF-319) were purchased from Microchem Corporation. Gold pellets (5 N purity, ESPI Metals) and chromium powder (3 N purity, American Elements) were used for the evaporation of films.

CdSe Nanowire Synthesis. CdSe nanowire arrays were prepared on glass slides by electrodeposition using the LPNE process as previously described.[43−45] Briefly, a 60 nm thick nickel film (ESPI, 5 N purity) was thermally evaporated onto clean 1 in. × 1 in. squares of soda lime glass. A positive photoresist (PR) layer (Shipley, S1808) was spin-coated (2500 rpm, 80 s), and a PR layer ≈800 nm in thickness was formed after soft-baking (90 °C, 30 min). The PR was then patterned using a quartz and chromium contact mask in conjunction with a flood exposure UV source (Newport model 97436 500W × 1.8 s) equipped with a photolithographic alignment fixture (Newport 83210). The exposed PR region was developed for 25 s (Shipley, MF-319), rinsed with Millipore water, and air-dried. Exposed nickel was removed by dipping the patterned samples in 0.8 M HNO_3 (Fisher, ACS Certified) solution for 6 min to create a horizontal trench with a typical width of 500 nm and a height that equaled the thickness of the evaporated nickel layer. The entire lithographically patterned region was then immersed in an aqueous plating solution with the exception of one edge where an electrical contact to the nickel layer was established with an alligator clip.

CdSe nanowires were then electrodeposited in the lithographically produced trench using the scanning electrodeposition/stripping method.[43−45] The potential of the nickel edge was scanned at 50 mV/s from an initial potential of −400 mV *vs* SCE to a negative scan limit of −800 mV and back. CdSe nanowires with a width of 400−450 nm were prepared using four voltammetric

scans in an unstirred aqueous plating solution (25 °C) with 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1−2.[60,94] (Caution: both $CdSO_4$ and SeO_2 are highly toxic.) Electrodeposition was carried out in a one-compartment, three-electrode electrochemical cell using a Gamry G300 potentiostat. After the CdSe electrodeposition was complete, the remaining PR was removed with acetone (Fisher, ACS Certified) and the remaining nickel was removed with 0.8 M HNO_3 solution by etching for 10 min. The removal of PR and nickel exposed the array of electrodeposited CdSe nanowires that were strongly adherent to the surface of the glass substrate. Either of two postdeposition thermal treatments were carried out: (1) As-deposited CdSe nanowires were heated in flowing N_2 at 300 °C for 4 h using a tube furnace (Lindberg, 54233) and then cooled to room temperature. (2) As-deposited CdSe nanowires were heated in flowing N_2 at 450 °C for 1 h using the same tube furnace.

Structural Characterization. Scanning electron microscopy (SEM) images were acquired using a Philips XL-30 FEG (field emission gun) SEM using an accelerating voltage of 10 keV. All samples were sputtered with a thin layer of Au/Pd prior to imaging to prevent charging. Grazing incidence X-ray diffraction patterns were obtained using a Rigaku Ultima III high-resolution X-ray diffractometer employing the parallel beam optics with a fixed incident angle of 0.30°. The X-ray generator was operated at 40 kV and 44 mA with Cu Kα irradiation. The JADE 7.0 X-ray pattern data processing software (Materials Data, Inc.) was used to analyze acquired patterns and estimate the respective grain diameter size. Raman spectra were collected using a Renishaw inVia Raman microscope equipped with the Easy Confocal optical system (spatial resolution less than 1 μm) using a 532 nm laser and a 2400 line/mm grating. An optical power of 50 mW was used in conjunction with an integration time of 30 s. WiRE 3 software was used to acquire the data and images.

Device Fabrication. The procedure for the fabrication of 0.60 μm gaps, shown schematically in Figure 3a, was as follows: After the electrodeposition of *nc*-CdSe nanowires on soda lime glass, a thin layer of Au/Cr (50/1 nm) was thermally evaporated across the entire surface, covering the nanowires. Cr was used here as an adhesion layer. A positive photoresist (PR) layer (Shipley, S1808) was then spin-coated (2500 rpm, 80 s), producing a PR layer of thickness ∼800 nm after soft-baking (90 °C, 30 min). The PR was then patterned using a quartz contact mask in conjunction with a UV light source (365 nm, 500 W, ×2 s) equipped with a photolithographic alignment fixture (Newport, 83210-V). The exposed PR region was developed for 25 s (Shipley, MF-319) and rinsed with Millipore water (Milli-Q, $\rho > 18\ \Omega\cdot$cm). The exposed Au and Cr were removed by dipping in $KI/I_2/H_2O$ (4/2/40 g) solution for 10 s and standard Cr etchant (Aldrich) for 3 s, respectively. The etching produced an undercut at the edges of the exposed PR. The second layer of Au/Cr (50/1 nm) was then thermally evaporated and removed from the PR-coated half of the device using lift-off. This produced a sub-micrometer gap with dimensions of approximately 0.60 μm.

Devices with 5 μm gaps between the gold contacts were prepared using conventional photolithography and lift-off as follows: After the electrodeposition of nanowires on the glass surface, a positive photoresist (PR) layer (Shipley, S1808) was spin-coated (2500 rpm, 80 s), and a PR layer of ∼800 nm thickness was formed after soft-baking (90 °C, 30 min). The photoresist was photopatterned using a quartz contact mask that defined a 5 μm gap. After developing the photoresist and rinsing the surface, a thin layer of Au/Cr (50/1 nm) was thermally evaporated. Finally, the 5 μm gap between contacts was created by gold lift-off.

Electrical Properties and Electroluminescence. Current−voltage characteristics of *nc*-CdSe were measured using a Keithley 2400 sourcemeter controlled by LabVIEW software. EL emission was recorded using an Olympus IX71 optical microscope equipped with an Andor Neo sCMOS CCD camera controlled by Andor SOLIS software. EL spectra were collected using a Spectra Pro 2300i spectrophotometer equipped with a 600 g/mm grating and Winspec software. These spectra were acquired by locating the nanowire array within a few millimeters of the entrance slit of the spectrophotometer. Kelvin probe force microscopy (KPFM) images were acquired using an Asylum Research, MFP-3D AFM equipped with Olympus, ASYELEC-01 tips coated with Ti/Ir (3/15) in a laboratory air ambient.

Conflict of Interest: The authors declare no competing financial interest.

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